Tutorial 5 - SS2021
Communication Systems and Protocols

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6

Task 1: I²C-Bus Synchronization

Three I²C Bus Masters want to send data to one slave. Each node needs one time step to read in data from external signal lines (SCL, SDA). The reaction time within each node is negligibly small (0 time steps). The individual masters want to establish a clock signal according to the following table 1.1:

Master	Low period	High period
A	8	4
B	4	12
C	12	8

Table 1.1: clock signals

Assume that Master B is initiating the communication cycle.

A) In general, which functionality does the I²C bus provide for the case that multiple master nodes want to communicate at the same time with the same slave node? **1**

The I²C-Bus uses clock synchronization and arbitration (over the complete dataframe, over address and data fields).

B) Complete the waveforms of the signals that result from the interaction between the nodes on the SCL signal. **3**

C) In general, which functionality does the I2C bus provide for the case when there is a fast and a slow master node? **2**

The I²C-Bus allows slower nodes to insert wait states if the other node is too fast. The wait state insertion is controlled by the SCL signal. In general, the SCL signal is generated by a wired-AND connection with dominant "LOW" of the participants CLK signals. A wait state is inserted if the SCL signal remains "LOW" and is initiated by a slower node.

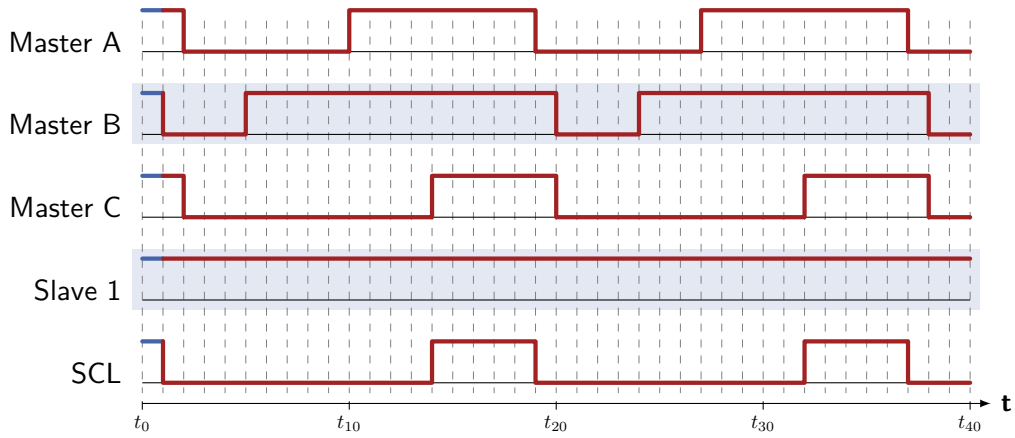

Figure 1.1: Signal sequence

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Task 2: Actuator Sensor Interface (ASI)

In the following a data transmission on the ASI bus is considered. Thereby a master wants to transmit the bit vector 01001 to the slave having address 26_d. The telegram format of the ASI bus is shown in Figure 2.1.

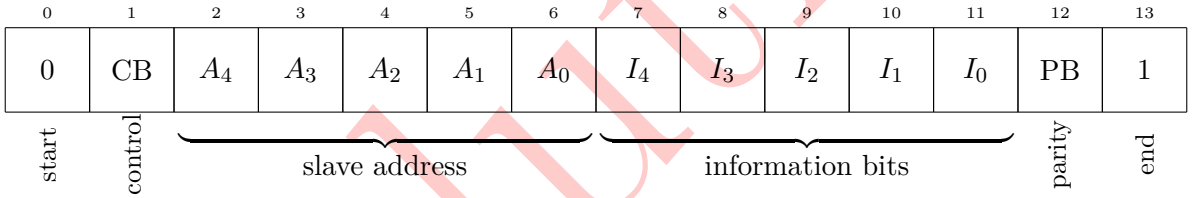

Figure 2.1: ASI packet format, master call

A) Specify the course of the sender voltage on the ASI bus. A time offset does not need to be considered (Note: The control bit must have value '0' for data transmission, use even parity without considering start / stop bits). Use figure 2.2 and Manchester as per IEEE 802.3

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B) Figure 2.3 shows the waveform on the ASI bus when transmitting a master call. Due to external influences the transmission has been disturbed. Mark the errors and name the rule(s) by which they are detected.

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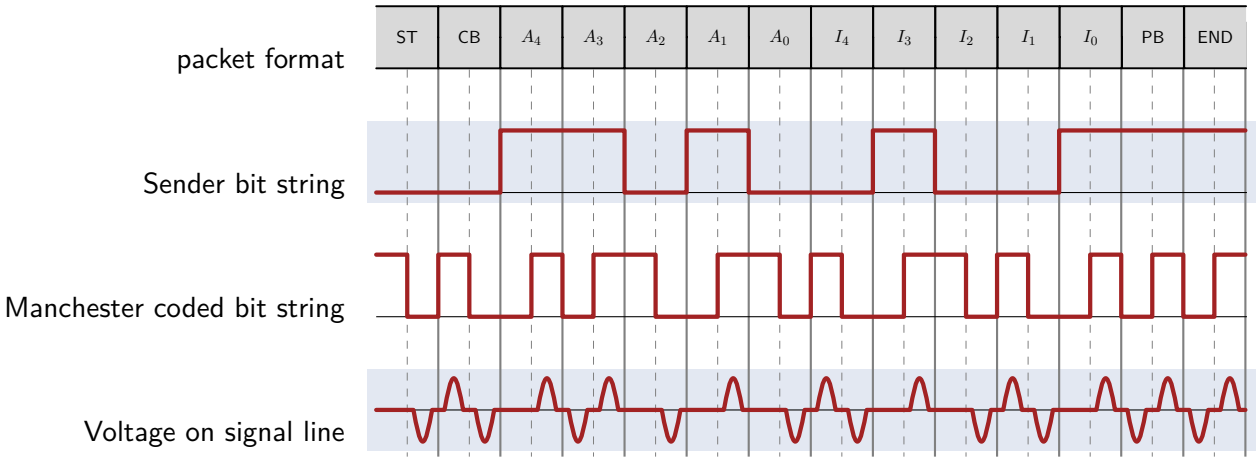

Figure 2.2: Waveform of the sender voltage

1. Start and stop bits: first impulse has to be negative, last impulse has to be positive
2. Succeeding impulses must have different polarity
3. Between two impulses of a telegram the pause that is allowed lasts half a bit time at maximum
4. The parity of the telegram must be even. In the example this cannot be seen since the transmitted data cannot be reconstructed due to the great amount of errors

Figure 2.3: Waveform of the sender voltage